Claim Amendments

1-5 (canceled).

6. (previously presented) A memory system comprising:

a memory comprising first and second groups of dynamic memory cells, each cell storing a bit;

an access circuit connected to the memory to access, during an access cycle, a selected one of:

a first set of the bits stored in said first group of said memory cells; and

a second set of the bits stored in said second group of said memory cells;

an error detection circuit connected to the access circuit and said memory to detect an error in a bit accessed during said access cycle, comprising:

a first error detection circuit to detect an error in a bit of said first set of accessed bits; and

a second error detection circuit to detect an error in a bit of said second set of accessed bits; and

a scrub circuit connected to the memory to scrub, during a scrub cycle, a selected one of:

said first set of the bits stored in said first group of said memory cells; and

said second set of the bits stored in said second group of said memory cells.

7. (original) The memory system of claim 6 wherein said first and second error detection circuits also correct said bit errors, respectively.

8. (original) The memory system of claim 6 wherein said first and second subsets of said accessed bits are comprised of equal numbers of said bits.

9. (original) The memory system of claim 6 wherein said first and second subsets of said accessed bits are comprised of different numbers of said bits.

10. (canceled).

11. (previously presented) The memory system of claim 6 wherein said access cycle and said scrub cycle are non-overlapping.

12. (previously presented) The memory system of claim 6 wherein said access cycle overlaps said scrub cycle, and wherein, during said access cycle, said access circuit accesses said selected one of said first and second sets of bits, and, during said scrub cycle, said scrub circuit scrubs the other of said selected first and second sets of bits.

13. (previously presented) The memory system of claim 6 wherein the memory system comprises an integrated circuit.

14. (previously presented) A memory system comprising:

a memory comprising a plurality of dynamic memory cells arranged in a plurality of planes of rows and columns, each cell storing a bit and corresponding memory cells of each plane forming respective stacks;

an access circuit connected to the memory to access, during said access sequence, all of the bits stored in all of said planes of said memory cells; and

an orthogonal error detection circuit connected to the access circuit and said memory to detect an error in a bit accessed during said access sequence, comprising:

a row error detection circuit to detect an error in a bit of a row of said accessed bits;

a column error detection circuit to detect an error in a bit of a column of said accessed bits; and

a stack error detection circuit to detect an error in a bit of a stack of said accessed bits.

15. (previously presented) The memory system of claim 14 wherein said first, second and third error detection circuits also correct said bit errors, respectively.

16. (cancelled).

17. (previously presented) The memory system of claim 14 wherein the stack error detection circuit comprises a parity check circuit.

18. (previously presented) The memory system of claim 14 wherein the stack error detection circuit comprises a RAEDAC unit.

19. (original) The memory system of claim 14 wherein the column error detection circuit comprises a parity check circuit.

20. (original) The memory system of claim 14 wherein the column error detection circuit comprises a RAEDAC unit.

21. (original) The memory system of claim 14 wherein the row error detection circuit comprises a parity check circuit.

22. (original) The memory system of claim 14 wherein the row error detection circuit comprises an EDAC unit.

23. (original) The memory system of claim 14 wherein the memory system comprises an integrated circuit.

24-37. (cancelled).